IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A multi-stage, multi-dimensional, credit-based, adaptive flow control switch comprising:

a plurality of first stage port processors, each one of the plurality of first stage port processors having an integrator block for receiving a token bit and updating a grant credit in response to receiving the token bit; ~~and~~

a plurality of second stage port processors connected to the plurality of first stage port processors for receiving data packets from the plurality of first stage port processors, each one of the plurality of second stage port processors having a statistics block coupled to a corresponding integrator block; and

a plurality of third stage port processors connected to the plurality of second stage port processors;

wherein the statistics block is further coupled to one or more neighboring integrator blocks for transmitting a token bit to the corresponding integrator block and the one or more neighboring integrator blocks, the statistics block transmitting the token bit in response to a second stage port processor associated with the statistics block receiving a data packet from one of the plurality of the first stage port processors;

wherein the statistic block further comprises a real-time counter for accumulating real-time statistics of data packet arrivals from one of the plurality of first stage port processors and data packet departures to one of the plurality of third stage port processors.

2. (original) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 1, wherein the corresponding integrator block includes an (i)th integrator block and the one or more neighboring integrator blocks include an (i-l)th integrator block that is located above the corresponding (i)th integrator block.

3. (original) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 2, wherein the one or more neighboring integrator blocks further include an (i+l)th integrator block that is located below the corresponding (i)th integrator block.

4. (original) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 3, wherein the one or more neighboring integrator blocks increase associated grant credits in response to receiving a token bit from the statistic block.

5. (original) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 4, wherein the corresponding integrator block decreases an associated grant credit in response to receiving a token bit from the statistic block.

6. (original) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 5, wherein the plurality of first stage port processors includes one or more input ports and one or more output ports, wherein the arriving data packet is received at one of the one or more input ports and routed to an output port having a maximum number of grant credit.

7. Cancelled

8. (Currently Amended) The multi-stage, multi-dimensional, credit-based adaptive flow control switch as claimed in claim [[7]] 1, wherein the switch further includes a relay from each one of the third stage port processors to the plurality of first stage port processors, and the token bit is transmitted to the first stage port processors by one of second stage port processor and the third stage port processor.

9. (original) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 8, wherein the plurality of first stage switch elements and the plurality of third stage switch elements are embedded on a single chip.

10. (Currently Amended) An adaptive filtering method for controlling traffic flow in a multi-stage, multi-dimensional, switched network, comprising:

notifying a plurality of first stage port processors in response to receiving a data packet from one of the plurality of first stage port processors, wherein the plurality of first stage port processors includes the one of the plurality of first stage port processors from which the data packet is received and at least one neighboring first stage port processor; ~~and~~

updating grant credits associated with said one of the plurality of first stage port processors and ~~one or more~~ the at least one neighboring first stage port ~~processors~~ processor in response to the notifying, wherein the updating grant credits comprises:

decrementing a grant credit associated with said one of the plurality of first stage port processors; and

incrementing one or more grant credits associated respectively with the one or more neighboring first stage port processors;

determining a port processor among the plurality of first stage port processors for forwarding an incoming data packet by selecting an output port processor having a maximum grant credit;

receiving the incoming data packet at the determined port processor; and

routing the data packet to a corresponding second stage port processor.

11. Cancelled

12. Cancelled

13. Cancelled

14. Cancelled

15. (original) The adaptive filtering method of claim 10, wherein the one or more neighboring first stage port processors include a first stage port processor coupled adjacent to said one of the plurality of first stage port processors.

16. (original) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 1, wherein the one or more neighboring integrator blocks change associated grant credits in response to receiving a token bit from the statistic block.

17. (original) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 1, wherein the corresponding integrator block change an associated grant credit in response to receiving a token bit from the statistic block.

18. (original) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch as claimed in claim 1, wherein the statistics block departs the data packet.

19. (Currently Amended) A multi-stage, multi-dimensional, credit-based, adaptive flow control switch comprising:

a plurality of first stage port processors[[,]] adapted for receiving a token bit and updating a grant credit in response to receiving the token bit, each first stage port processor including one or more input ports and one or more output ports; and

a plurality of second stage port processors connected to the plurality of

first stage port processors for receiving data packets from the plurality of first stage port processors; and

a plurality of third stage port processors connected to the plurality of second stage port processors;

wherein each one of the plurality of second stage port processors ~~having~~ includes a statistics block adapted to transmit the token bit in response to a second stage port processor associated with the statistics block receiving a data packet from an output port of one of the plurality of the first stage port processors having a maximum number of grant credits;

wherein the statistic block further comprises a real-time counter for accumulating real-time statistics of data packet arrivals from one of the plurality of first stage port processors and data packet departures to one of the plurality of third stage port processors.

20. (previously presented) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch of claim 19, wherein each one of the plurality of first stage port processors further comprises an integrator block that performs the receiving and updating functions.

21. (previously presented) The apparatus of claim 20, wherein each of the statistics blocks are further coupled to a corresponding integrator block and to one or more neighboring integrator blocks.

22. (previously presented) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch of claim 21, wherein the corresponding integrator block includes an (i)th integrator block and the one or more neighboring integrator blocks include an (i-l)th integrator block that is located above the corresponding (i)th integrator block.

23. (previously presented) The multi-stage, multi-dimensional, credit-

based, adaptive flow control switch of claim 22, wherein the one or more neighboring integrator blocks further include an (i+l)th integrator block that is located below the corresponding (i)th integrator block.

24. (previously presented) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch of claim 21, wherein the one or more neighboring integrator blocks change associated grant credits in response to receiving a token bit from the statistic block.

25. (previously presented) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch of claim 24, wherein the one or more neighboring integrator blocks increase associated grant credits in response to receiving a token bit from the statistic block.

26. (previously presented) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch of claim 21, wherein the corresponding integrator block changes an associated grant credit in response to receiving a token bit from the statistic block.

27. (previously presented) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch of claim 26, wherein the corresponding integrator block decreases an associated grant credit in response to receiving a token bit from the statistic block.

28. Cancelled

29. (Currently Amended) The multi-stage, multi-dimensional, credit-based adaptive flow control switch of claim [[28]] 19, wherein the switch further includes a relay from each one of the third stage port processors to the plurality of first stage port processors, and the token bit is transmitted to the first stage

port processors by one of second stage port processor and the third stage port processor.

30. (Currently Amended) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch of claim [[28]] 19, wherein the plurality of first stage port processors and the plurality of third stage port processors are embedded on a single chip.

31. Cancelled

32. Cancelled

33. Cancelled

34. Cancelled

35. Cancelled

36. (previously presented) The multi-stage, multi-dimensional, credit-based, adaptive flow control switch of claim 19, wherein the statistics block departs the data packet.